4.5V~100V, 3.5A Peak, Asynchronous, DC-DC Step-Down Converter

CJ92930 **DC-DC**

1 Introduction

The CJ92930 is a 100V/3.5A peak switching current limit, asynchronous buck converter which integrates a high-side power MOSFET Utilizing of advanced COT control method reduces the size of the total solution and achieves excellent load transient performance. The integrated BST charge circuit minimizes both cost and solution size. High duty Ton extension feature makes it ideal for applications that requiring low drop-out voltage. 190μA quiescent current saves the power, and only 3uA low off-current makes it suitable for battery powered applications.

The CJ92930 is available in a cost- effective ESOP8 package.

2 Available Packages

PART NUMBER	PACKAGE
CJ92930	ESOP8

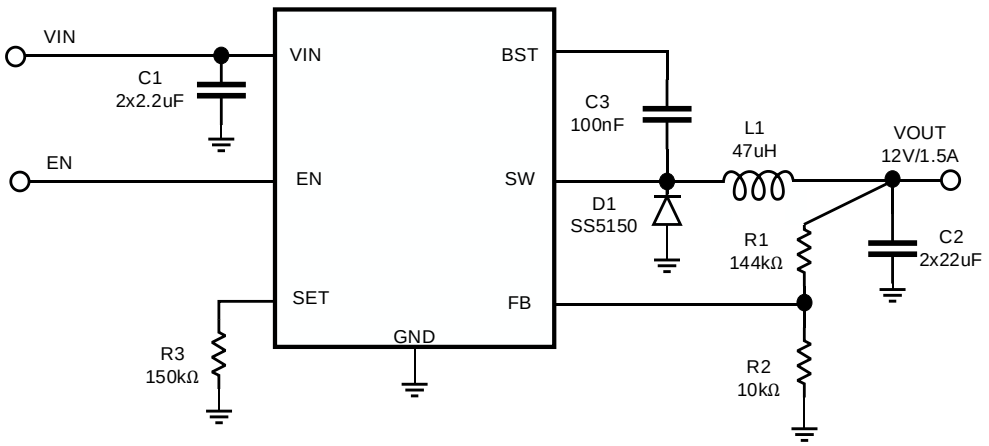
3 Features

- 4.5V to 100V Wide Input Range
- 3.5A Typical Peak Current Limit
- Integrated 500mΩ Low Resistance High Side Power MOS
- Constant On Time Control with Constant Switching Frequency.
- 190μA Low Quiescent Current
- Selectable 150/240/420kHz Switching Frequency
- Special Valley Current Limit for Asynchronous Buck Short Circuit Protection
- 3μA Low Current at Off-State
- Built-in Pull-Up Current at EN Pin
- Available in ESOP8 Package

4 Applications

- Battery powered tools
- E-bike powers, E-motors
- Industry applications

Typical Application



5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ92930-PBN	ESOP8	-40 ~ 125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:

Active: Recommended for new products.

Customized: Products manufactured to meet the specific needs of customers.

Preview: The device has been released and has not been fully mass produced. The sample may or may not be available.

NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers.

Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

ESOP8

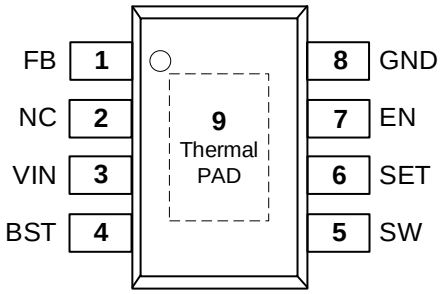


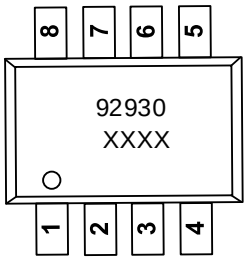
Figure 6-1 Pin Configuration

6.2 Pin Function

PIN		I / O(1)	DESCRIPTION
No.	NAME		
1	FB	I	Feedback. Connect a resistor divider to set the output voltage.
2	NC	-	No Connected
3	VIN	P	Supply input terminal to internal bias LDO and high-side FET. Connect to input supply and input bypass capacitors CIN. Input bypass capacitors must be directly connected to this pin and GND.
4	BST	P	Bootstrap capacitor connection for high-side FET driver. Connect a high quality 100nF capacitor from this pin to the SW pin.
5	SW	P	Switching node of power stage. Connect to power inductor.
6	SET	I	Switching frequency selection pin.
7	EN	I	Enable of the part. Pull down this pin to shut down the part. Internally pulled up by current source.
8	GND	G	Ground pin of IC. Connect to the ground of the system.
9	EP	-	Exposed Pad. Connect exposed pad to the PCB GND plane to achieve good thermal performance.

(1) I-Input, O-Output, P-Power, G-Ground

6.3 Marking Information



"92930": Device code.
"XXXX": Date Code.

7 Specifications

7.1 Absolute Maximum Ratings

(T_A = 25°C, unless otherwise specified) (1)

SYMBOL	CHARACTERISTIC	VALUE	UNIT
V_{IN}	VIN to GND	-0.3 ~ 105	V
V_{SW}	SW to GND	-0.3 ~ 105	V
V_{BST} - V_{SW}	BST to SW	5.5	V
I_{EN}	Max Input current to EN pin	100	uA
	All other input	-0.3 ~ 5.5	V
TJ	Junction temperature	-40 ~ 150	°C
Tstg	Storage temperature	-55 ~ 150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

Over operating ambient temperature range (unless otherwise noted)

SYMBOL	PARAMETER	MIN.	NOM.	MAX.	UNIT
V_{IN}	VIN to GND	4.5		100	V
V_{OUT}	V_{OUT} to GND	0.8		V_{IN}*D_{MAX}(1) Or 28	V
I_{OUT}	Continuous Output Current (V_{OUT}=12V)	0		1.5	A
I_{OUT}	Continuous Output Current (V_{OUT}=5V)	0		2	A
I_{OUT}	Transient Output Current	0		3	A

(1) D_{MAX} = T_{ON_MAX} /(T_{ON_MAX} + T_{OFF_MIN}). Typical value is 97%.

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM) (1)	±2000	V
$V_{ESD-CDM}$		Charged-device model (CDM) (2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.4 Thermal Information

SYMBOL	THERMAL METRIC	ESOP8	UNIT
$R_{\Theta JA}$(1)	Junction-to-ambient thermal resistance	42.9	℃/W
$R_{\Theta JC(top)}$(1)	Junction to case (top) thermal resistance	54	℃/W
$R_{\Theta JB}$(1)	Junction-to-board thermal resistance	13.6	℃/W

(1) The value given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were measured on JESD 51-7, 4-layer JEDEC PCB board.

7.5 Electrical Characteristics

V_{IN}=60V and T_A=25°C, unless otherwise specified.

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIN_{UV_R}	VIN UVLO rising voltage			4.3		V
VIN_{UV_F}	VIN UVLO falling voltage			4		V
VIN_{UV_HYS}	Hysteresis voltage of VIN UVLO			0.3		V
I_S	Shut down current from VIN	V_{EN}=0V		3		μA
I_Q	Quiescent current from VIN	V_{FB}=0.85V		190		μA
V_{EN_R}	Enable rising voltage			1.2		V
V_{EN_F}	Enable falling voltage			1		V
$I_{EN\_PULL\_UP}$	Enable pull-up current	V_{EN}=Low		1		μA
		V_{EN}=High		4		μA
$V_{ENCLAMP}$	EN clamp voltage	EN voltage at 100μA current		5.7		V
V_{FB}	Feedback voltage		0.768	0.78	0.792	V
V_{FB_UV}	Feedback voltage under voltage threshold			0.1		V
R_{HS_ON}	High Side power MOS ON resistance	V_{BST}-V_{SW}=5V		500		mΩ
I_{LIMIT_HS}	High side current limit threshold			3.5		A
T_{SS}	Soft-start time	V_{FB} from 10% to 90%		1.8		ms
F_{SW}	Switching frequency	SET floating		420		kHz
		R_{SET}=150k		240		kHz
		R_{SET}=75k		150		kHz
T_{ON_MIN} (1)	Min on time			150		ns
T_{ON_MAX}	Max on time			10		μs
T_{OFF_MIN} (1)	Min off time			320		ns
T_{OTP_R} (1)	Thermal shutdown entry threshold			160		°C
T_{OTP_F} (1)	Thermal shutdown recovery threshold			140		°C

(1) Guaranteed by design and engineering sample characterization

8 Detailed Description

8.1 Overview

The CJ92930 is a 100V/3.5A peak switching current limit, asynchronous buck converter which integrates a high-side power MOSFET Utilizing of advanced COT control method reduces the size of the total solution and achieves excellent load transient performance. The integrated BST charge circuit minimizes both cost and solution size. High duty Ton extension feature makes it ideal for applications that requiring low drop-out voltage. 240μA quiescent current saves the power, and only 3uA low off-current makes it suitable for battery powered applications.

8.2 Functional Block Diagram

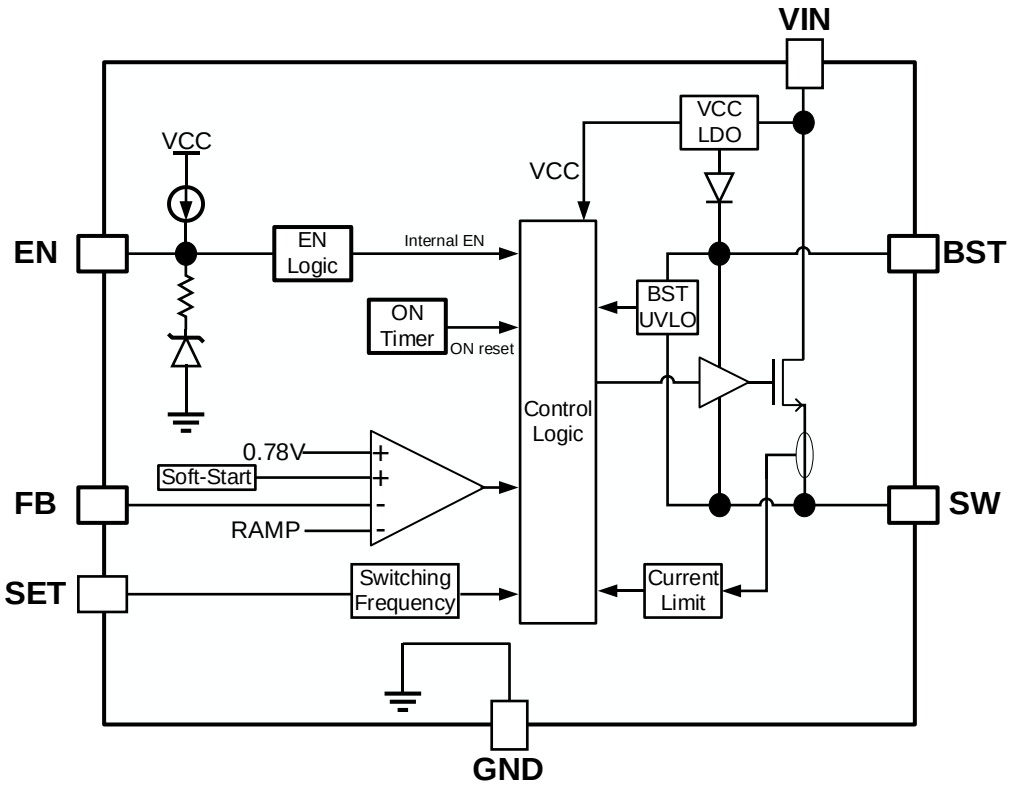


Figure 8-1 Function block diagram

8.3 Feature Description

8.3.1 Pulse-Width Modulation (PWM) Operation

The CJ92930 is a fully integrated, synchronous, step-down, switch-mode converter. It employs constant-on-time (COT) control to provide fast transient response and simplify loop stabilization. The high-side MOSFET (HS-FET) is turned on when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates an insufficient output voltage. The on-time is determined by both the output and input voltage, keeping the switching frequency relatively constant over the input voltage range. After the on-time elapses, the HS-FET is turned off and will turned on again when V_{FB} drops below V_{REF}. This repeated operation regulates the output voltage.

Internal compensation is applied for COT control to ensure more stable operation, even when ceramic capacitors are used as output capacitors. This internal compensation enhances jitter performance without affecting line or load regulation.

8.3.2 Heavy-Load Operation

When the output current is high and the inductor current remains above zero amps (see Figure 8-2), converter operates in Continuous conduction mode (CCM). The HS-FET is turned on for a fixed interval determined by the one-shot on-timer once the V_{FB} is below V_{REF}. After this interval, the HS-FET is turned off and the external free-wheeling

diode will handle the current.

In CCM operation mode, the switching frequency remains relatively constant, which is referred to as pulse-width modulation (PWM) mode.

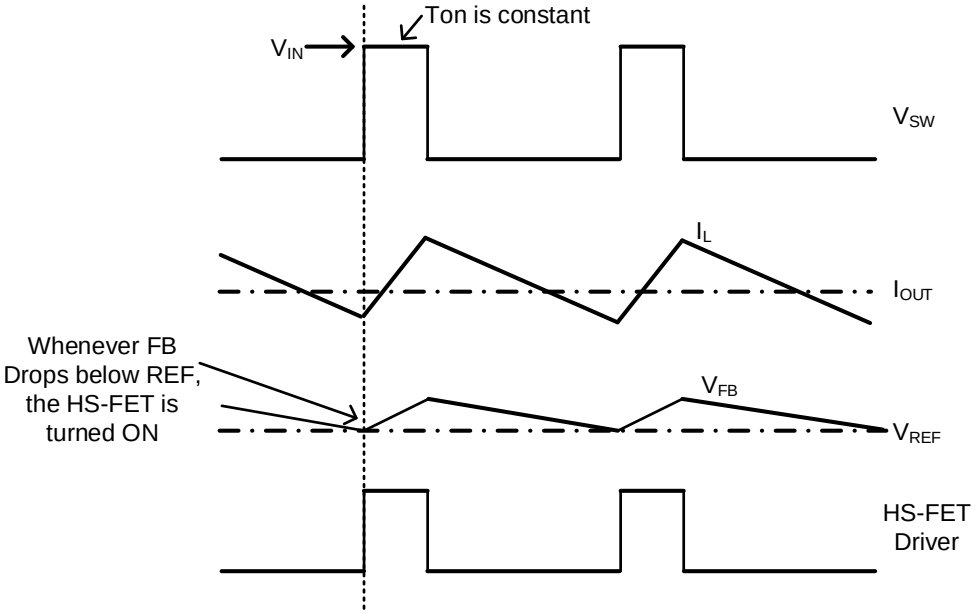


Figure 8-2 Heavy-Load Operation

8.3.3 Light-Load Operation

When the load decreases, the inductor current decreases as well. Once the inductor current reaches zero, the operation transitions from CCM to discontinuous conduction mode (DCM).

Light-load operation is shown in Figure 8-3. When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval determined by the one-shot on- timer. When the HS-FET is turned off, the free-wheeling diode is turned on until the inductor current drops to zero. In DCM operation, V_{FB} cannot reach V_{REF} while the inductor current is approaching zero. When the free-wheeling diode current arrives zero, it will shut down the negative current and SW goes into tri-state. The output capacitors are only discharged to GND through the feedback resistor slowly. As a result, the efficiency in light-load condition is improved greatly. In light-load condition, the HS-FET is not turned on as frequently as in heavy-load condition. This is called skip mode.

At light-load or no-load condition, the output drops very slowly, and the CJ92930 reduces the switching frequency naturally. High efficiency is achieved at light load.

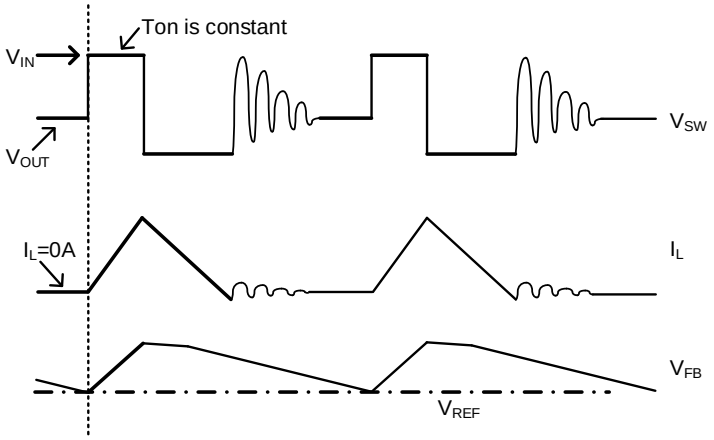


Figure 8-3 Light-Load Operation

As the output current increases from the light-load condition, the HS-FET is turned on more frequently, and the

switching frequency increases accordingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current can be determined with Equation (1):

$$\mathbf{I}_{OUT\_Critical} = \frac{(V_{IN}-V_{OUT})\times V_{OUT}}{2\times L\times f_{SW}\times V_{IN}} \quad (1)$$

The device enters PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains relatively constant over the output current range.

8.3.4 Enable (EN) Control

The CJ92930 has a dedicated enable control pin with positive logic. To turn on the regulator, drive the EN pin voltage higher than 1.2V(typical). To turn it off, drive the EN pin voltage lower than 1V (typical).

The EN pin includes an internal pull-up current source, allowing the CJ92930 to automatically startup when the EN pin is floating. More than 4μA pulldown current is required to shut down the regulator via EN pin. Once the EN pin is pulled low, its internal pull-up current will decrease to 1μA to reduce the shutdown current.

By using the two external resistor dividers, it is easy to optimize the system's start and stop voltage via EN pin:

Start voltage setting:

$$V_{START} = 1.2 \times \frac{R_{ENUP}+R_{ENDN}}{R_{ENDN}} - 1uA \times R_{ENUP} \quad (2)$$

Stop voltage setting:

$$V_{STOP} = 1 \times \frac{R_{ENUP}+R_{ENDN}}{R_{ENDN}} - 4uA \times R_{ENUP} \quad (3)$$

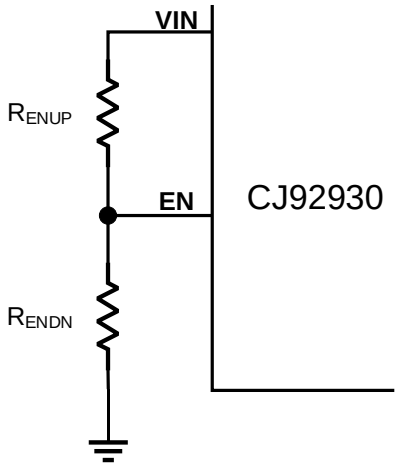


Figure 8-4 EN divider for adjustable UVLO

8.3.5 Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The CJ92930's UVLO comparator monitors the input voltage with 4.3V rising threshold and 4.05V falling threshold.

8.3.6 Internal Soft Start (SS)

Soft start (SS) prevents the output voltage from overshooting during start-up. When the chip starts, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up from 0V to 1V. When V_{SS} is below V_{REF}, V_{SS} overrides V_{REF}, the error amplifier uses V_{SS} as the reference. Once V_{SS} exceeds V_{REF}, the error amplifier switches to using V_{REF} as the reference. The SS time is set to 1.8ms internally.

8.3.7 Switching Frequency Set

The SET PIN can determine the switching frequency. The CJ92930 offers three options for switching frequency: 150KHz, 240KHz, and 420KHz. Selecting the switching frequency can be done by choosing the resistance value of the resistor connected between SET and GND. See the table below:

Table 1 Switching frequency set resistor selection

SET	Switching Frequency
SET Pin float	420kHz
R_{SET} = 18.7kΩ	240kHz
R_{SET} = 37.4kΩ	150kHz

8.3.8 Current Limit and Short Protection

The CJ92930 has a peak current limit and a special valley current limit circuit. During HS-FET on phase, the inductor current is monitored. If the sensed inductor current reaches the peak current limit after the blanking time, the HS-FET will be turned off. Due to the peak current limit's blanking time, the inductor current might runaway when output shorts to ground for an asynchronous buck. The special valley current limit in CJ92930 can prevent this failure. When HS-FET is off and the inductor current is larger than the valley current limit, the HS-FET remains off until the output current drops below the valley current limit threshold. As a result, CJ92930 will automatically fold back the switching frequency to prevent the current from running away, making the system more reliable.

8.3.9 Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, the entire chip shuts down. The chip recovers when the temperature falls below its lower threshold (typically 140°C).

9 Application and Implementation

9.1 Typical Application Circuit

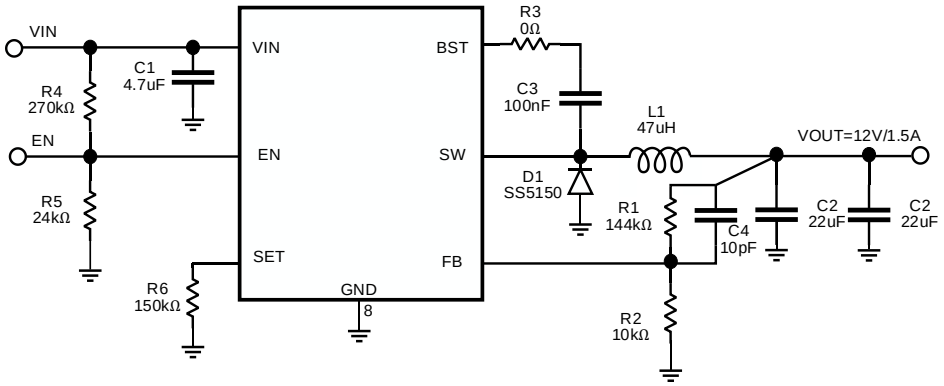


Figure 9-1 VIN=48V, VOUT=12V/1.5A, F_{SW}=240KHz

9.2 Component Selection

9.2.1 Setting the Output Voltage

The CJ92930 output voltage can be set by the external resistor dividers. The reference voltage is fixed at 0.78V. The feedback network is shown below Figure.

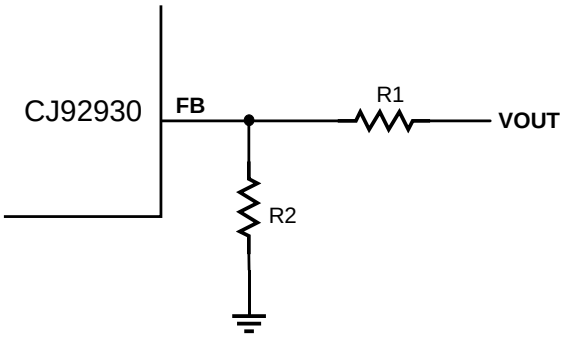


Figure 9-2 Feedback Network

Choose R1 and R2 using Equation:

$$V_{OUT} = V_{FB} \times \frac{(R1+R2)}{R2} \quad (4)$$

9.2.2 Selecting the Inductor

An inductor is necessary for providing a constant current to the output load while being driven by the switched input voltage. A larger-value inductor results in less ripple current and a lower output ripple voltage, but it also has a larger physical footprint, higher series resistance, and lower saturation current.

For most designs, the inductance value can be derived from the following Equation:

$$\mathrm{L} = \frac{(V_{IN}-V_{OUT})\times V_{OUT}}{\Delta I_L \times f_{SW} \times V_{IN}} \quad (5)$$

Where ∆IL is the inductor ripple current.

Select the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated using the following Equation:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (6)$$

Table 2 lists the recommended feedback resistor values for common output voltages.

Table 2: Resistor Selection for Common Output Voltages (1)

VOUT (V)	R1 (kΩ)	R2 (kΩ)	Cff(pF)	L (μH)	COUT(μF)
12	144	10	10	47	2x22
5	54	10	47	33	2x22

(1) For a detailed design circuit, please refer to the Typical Application Circuit

9.2.3 Selecting the Output Capacitor

The output capacitor maintains the DC output voltage ripple. Ceramic, tantalum, or low-ESR electrolytic capacitors can be used. For best results, use low ESR capacitors to minimize the output voltage ripple. The output voltage ripple can be estimated with Equation:

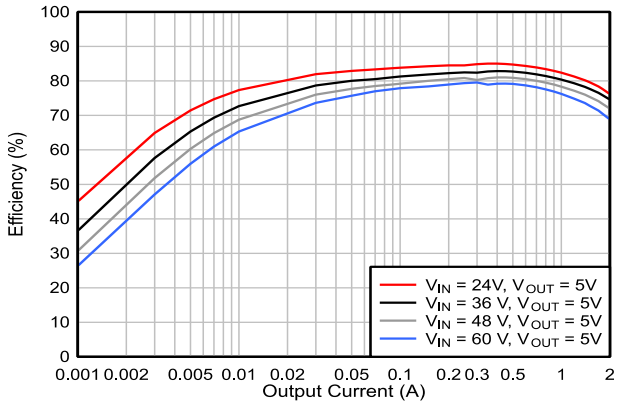
$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (7)$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

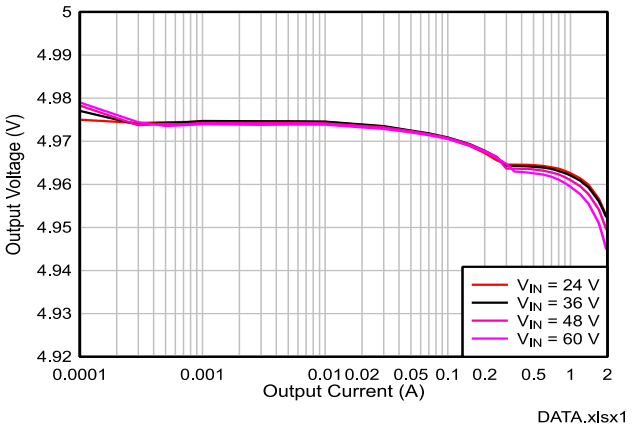
The characteristics of the output capacitor also affect the stability of the regulation system. The CJ92930 can be optimized for a wide range of capacitance and ESR values.

9.3 Application Curve

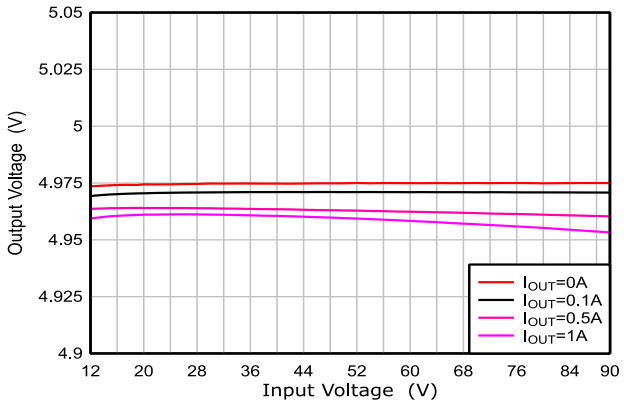
V_{IN} = 48V, V_{OUT} = 5V, C_{IN} = 2x2.2μF, C_{OUT} = 2x22μF, L1 = 33μH, and T_A = +25°C, unless otherwise noted.



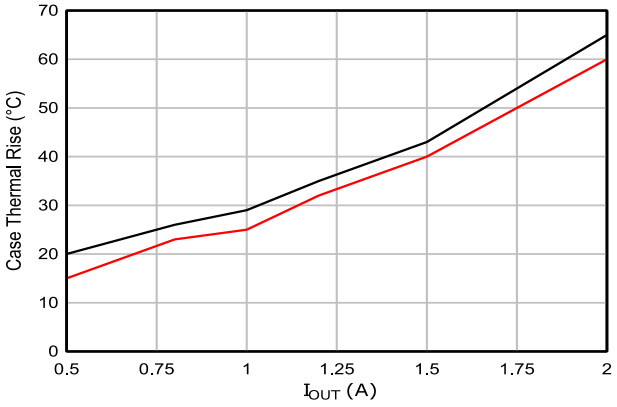
Efficiency vs. Load Current
(VOUT= 5V, F_{SW}=240KHz)



Load Regulation
(VOUT= 5V, F_{SW}=240KHz)

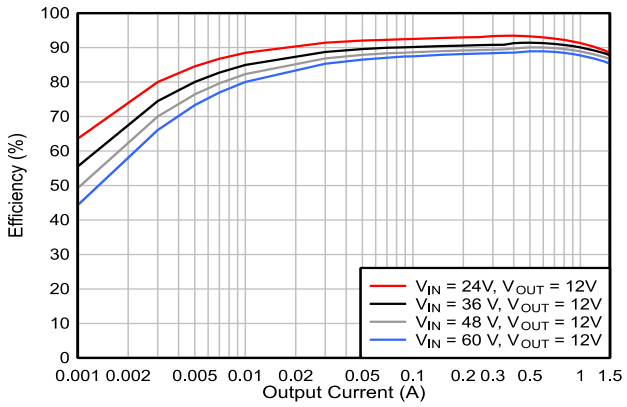


Line Regulation
(VOUT= 5V, F_{SW}=240KHz)

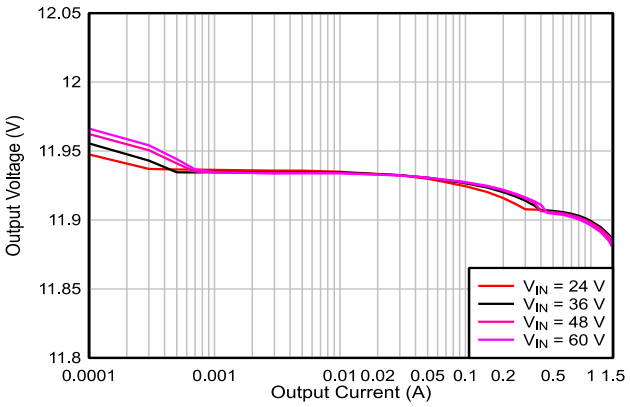


Thermal Rise
((VOUT= 5V, F_{SW}=240KHz, no air flow)

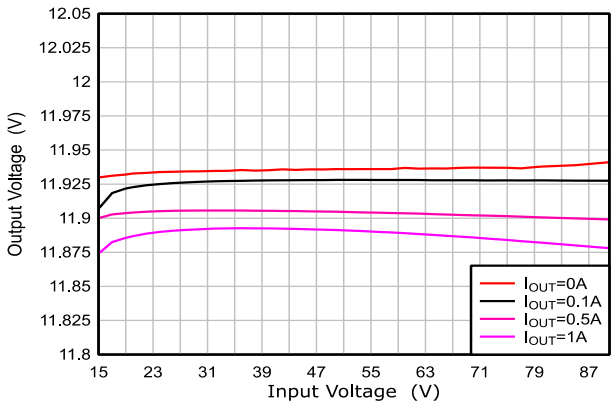
V_{IN} = 48V, V_{OUT} = 12V, C_{IN} = 2x2.2μF, C_{OUT} = 2x22μF, L1 = 47μH, and T_A = +25°C, unless otherwise noted.



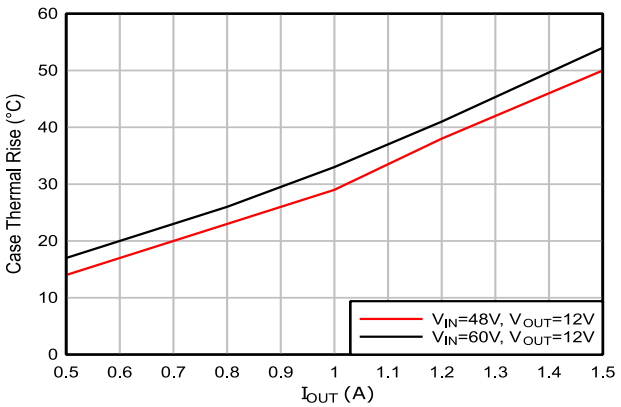
Efficiency vs. Load Current
(VOUT= 12V, F_{SW}=240KHz)



Load Regulation
(VOUT= 12V, F_{SW}=240KHz)

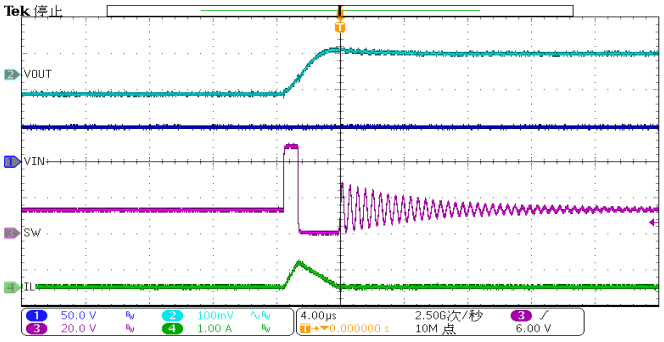


Line Regulation
(VOUT= 12V, F_{SW}=240KHz)

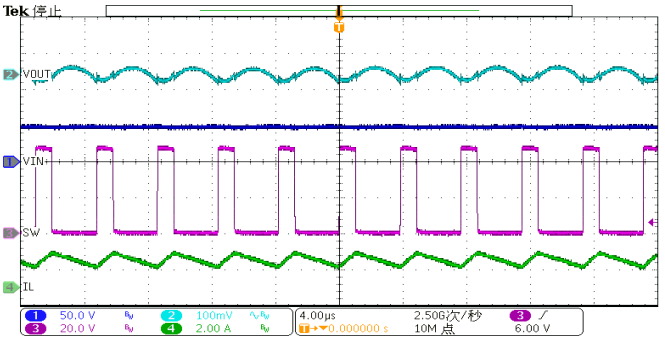


Thermal Rise
((VOUT= 12V, F_{SW}=240KHz, no air flow)

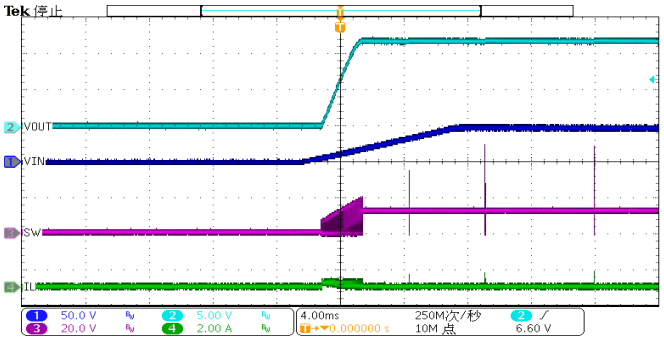
V_{IN} = 48V, V_{OUT} = 12V, C_{IN} = 2x2.2μF, C_{OUT} = 2x22μF, L1 = 47μH, and T_A = +25°C, unless otherwise noted.



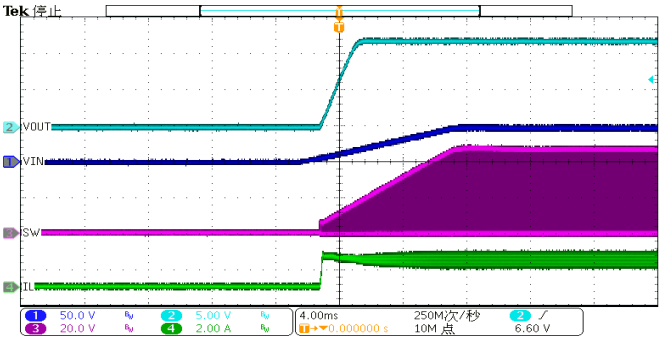
Output Voltage Ripple (I_{OUT}=0A)



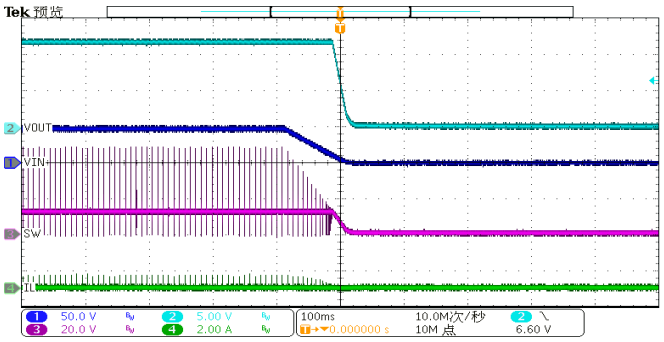
Output Voltage Ripple (I_{OUT}=1.5A)



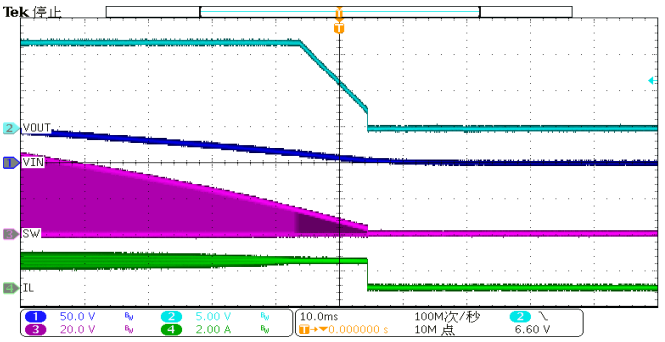
Start-Up through V_{IN} (I_{OUT}=0A)



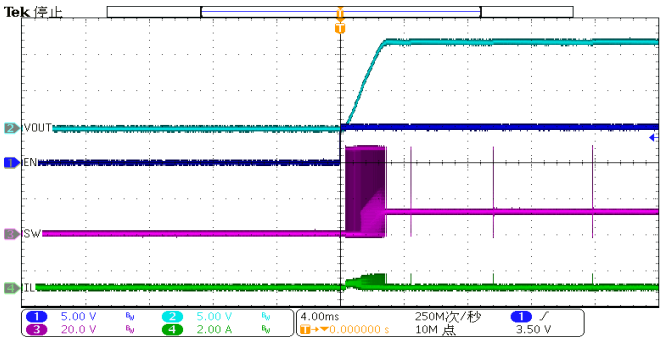
Start-Up through V_{IN} (I_{OUT}=1.5A)



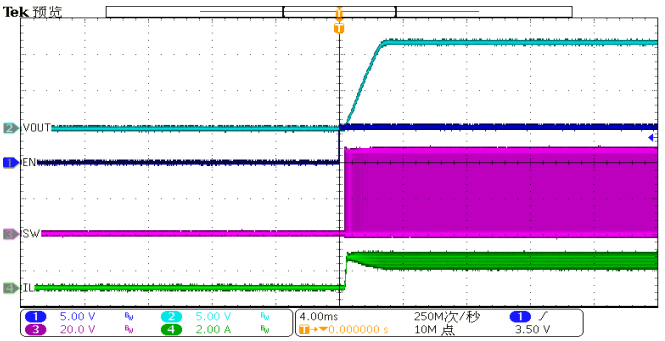
Shut-Down through V_{IN} (I_{OUT}=0A)



Shut-Down through V_{IN} (I_{OUT}=1.5A)

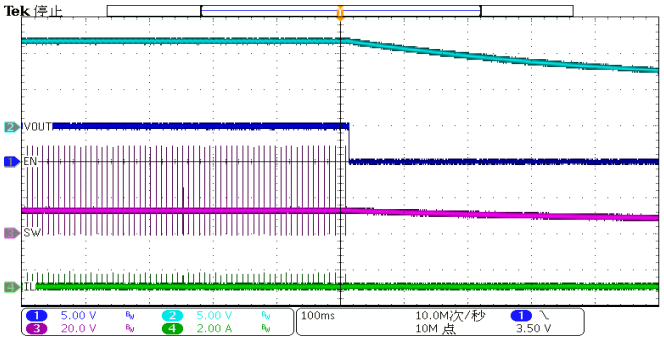


Start-Up through EN (I_{OUT}=0A)

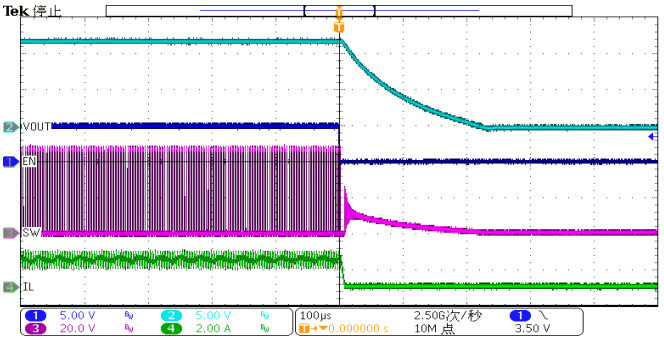


Start-Up through EN (I_{OUT}=1.5A)

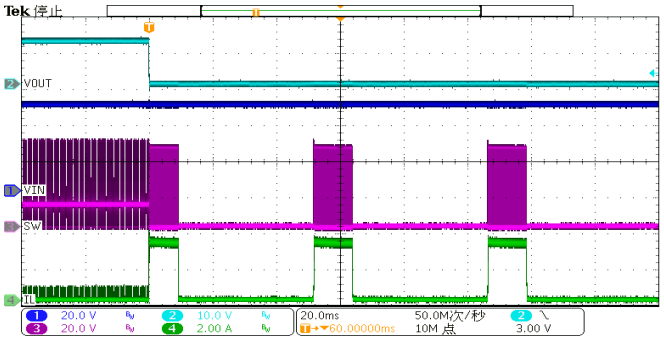
V_{IN} = 48V, V_{OUT} = 12V, C_{IN} = 2x2.2μF, C_{OUT} = 2x22μF, L1 = 47μH, and T_A = +25°C, unless otherwise noted.



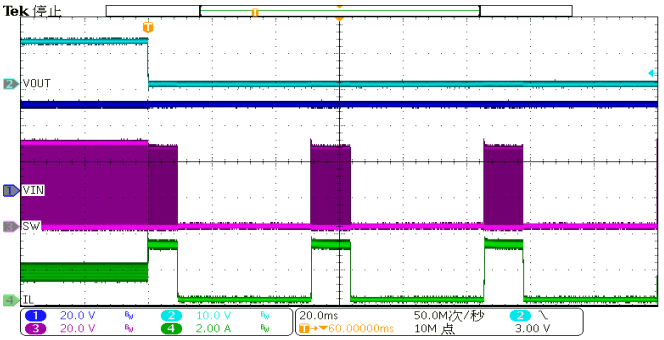
Shut-Down through EN (I_{OUT}=0A)



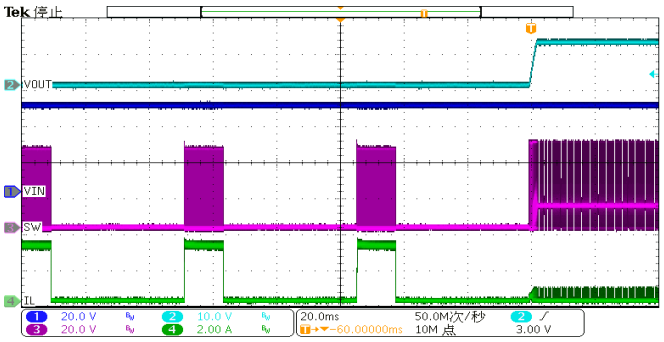
Shut-Down through EN (I_{OUT}=1.5A)



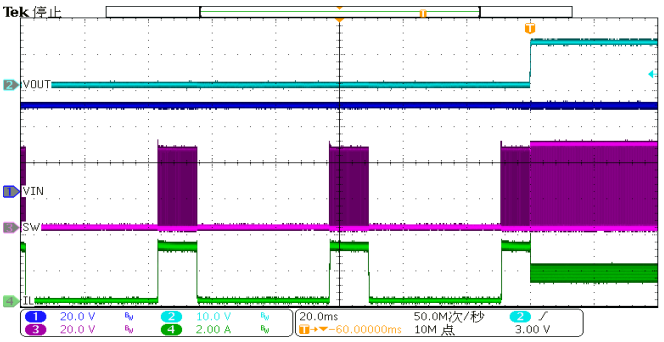
Short-Circuit Entry (I_{OUT}=0A)



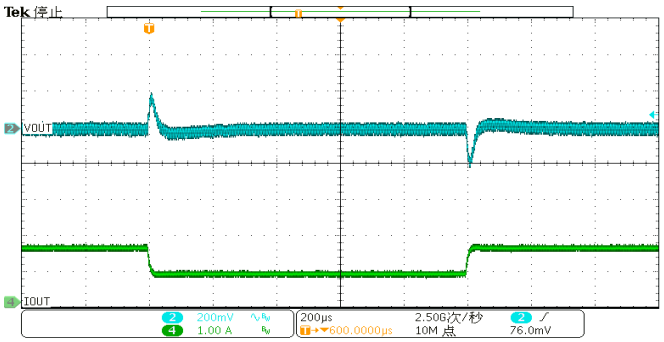
Short-Circuit Entry (I_{OUT}=1.5A)



Short-Circuit Recovery (I_{OUT}=0A)



Short-Circuit Recovery (I_{OUT}=0A)



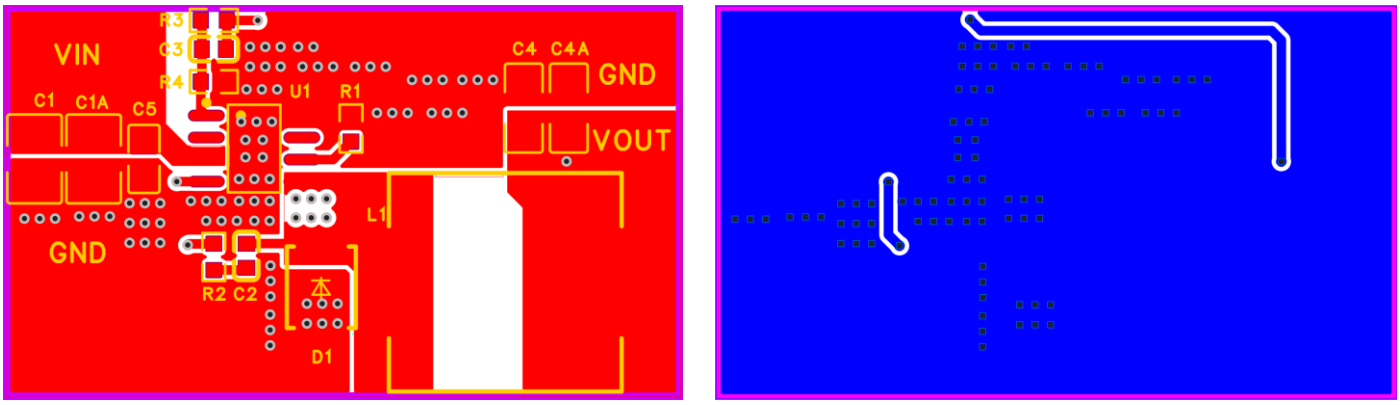
Load Transient
(V_{OUT} = 12V, L=47uH,
I_{OUT} = 0.75A to 1.5A, 2.5A/μs slew rate)

10 Layout

10.1 Layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation. For the high frequency switching converter, poor layout design may cause poor line or load regulation and stable issues. For best results, refer to below figure and follow the guidelines below.

- Place the input capacitor as close to VIN and GND as possible.
- Place the external feedback resistors as close to FB as possible.
- Keep the switching node (such as SW, BST) far away from the feedback network.
- Add a grid of thermal vias under the exposed pad to improve thermal conductivity.
- Minimize the power loop area formed by the input capacitor, IC, freewheeling diode, inductor and output capacitor.



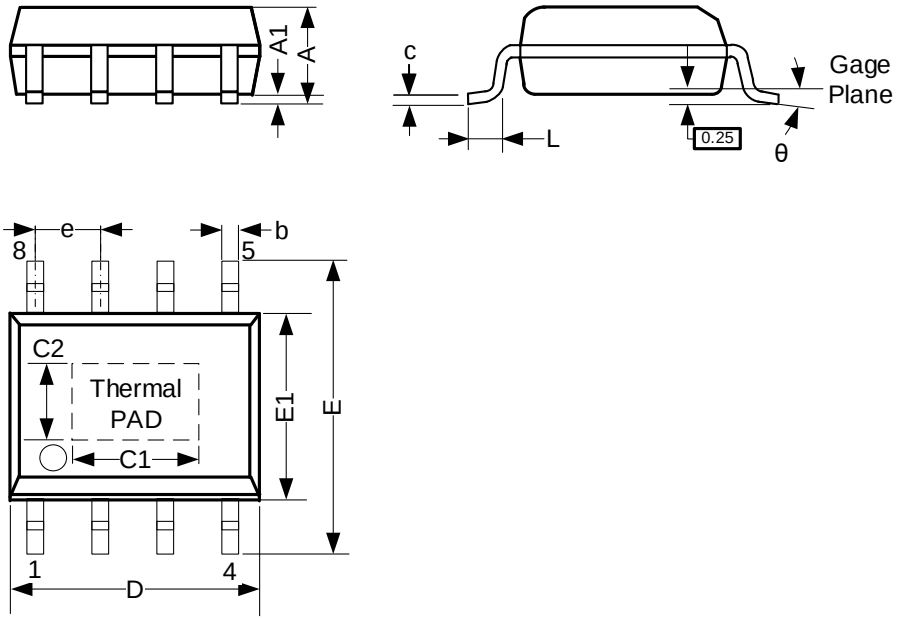
Top Layer Bottom Layer

Figure 10-1 Recommend PCB Layout

11 Mechanical Information

11.1 ESOP8 Mechanical Information

ESOP8 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.30	–	1.70
A1	0.00	–	0.15
b	0.33	–	0.51
c	0.19	–	0.25
C1	3.15	–	3.45
C2	2.26	–	2.56
D	4.80	–	5.00
E	5.80	–	6.20
E1	3.80	–	4.00
e	1.27 BSC		
L	0.41	–	1.27
θ	0°	–	8°

12 Notes

12.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

12.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

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